



YJL3400A

Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250	30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =30V, V _{GS} =0V			1	
Gate-Body Leakage Current	I _{GSS1}	V _{GS} = 12V, V _{DS} =0V			100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D =250	0.65	0.9	1.5	V
Static Drain-Source On-Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =5.6A		20	25	m
		V _{GS} =4.5V, I _D =5A		23	31	
		V _{GS} =2.5V, I _D =3A		27	45	
Diode Forward Voltage	V _{SD}	I _S =5.6A, V _{GS} =0V			1.2	V
Dynamic Parameters						
Input Capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V, f=1MHZ		630		pF
Output Capacitance	C _{oss}			55		
Reverse Transfer Capacitance	C _{rss}			71		
Switching Parameters						
Total Gate Charge	Q _g	V _{GS} =10V, V _{DS} =15V, I _D =5.6A		17.25		nC
Gate-Source Charge	Q _{gs}			2.1		
Gate-Drain Charge	Q _{gd}			2		
Reverse Recovery Charge	Q _{rr}	I _F =5.6A, di/dt=100A/us		1.1		
Reverse Recovery Time	t _{rr}			13.1		
Turn-on Delay Time	t _{D(on)}	V _{GS} =10V, V _{DS} =15V, I _D =5.6A R _{GEN} =		4.4		ns
Turn-on Rise Time	t _r			28.2		
Turn-off Delay Time	t _{D(off)}			16.2		
Turn-off fall Time	t _f			26		

A. Pulse Test: Pulse Width 300us, Duty cycle 2%.

B. R_{JA} is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{JC} is guaranteed by design, while R_{JA} is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.



Typical Performance Characteristics

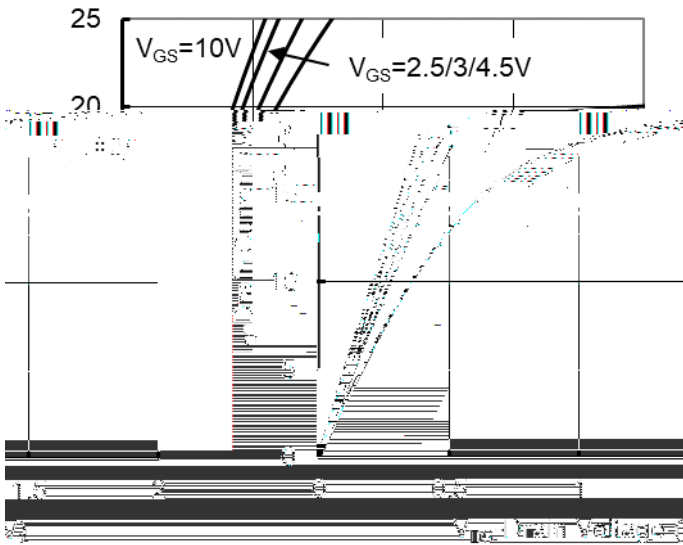


Figure1. Output Characteristics

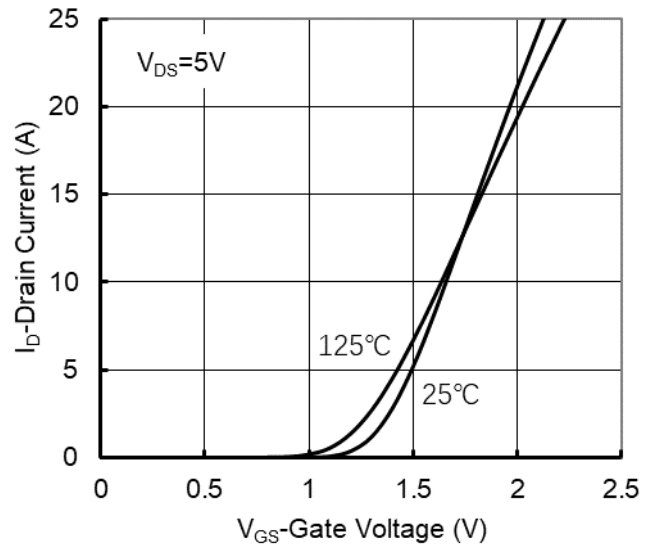


Figure2. Transfer Characteristics

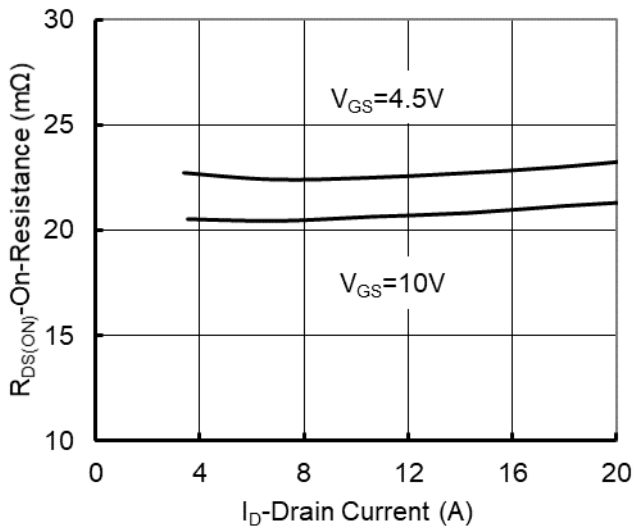


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

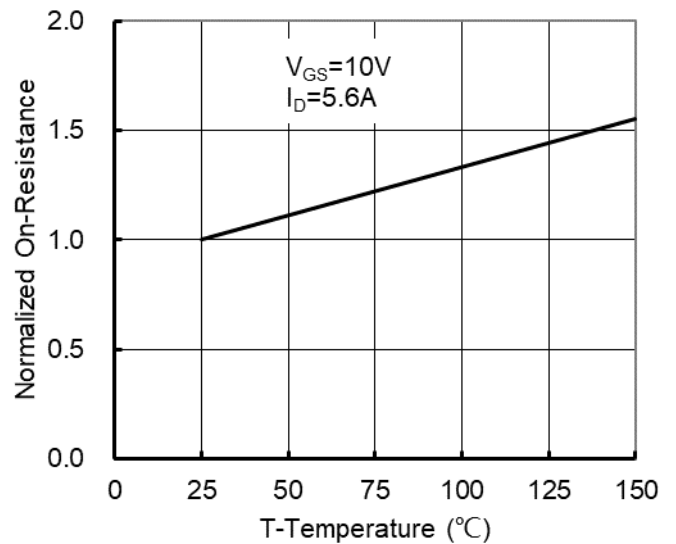


Figure 4: On-Resistance vs. Junction Temperature

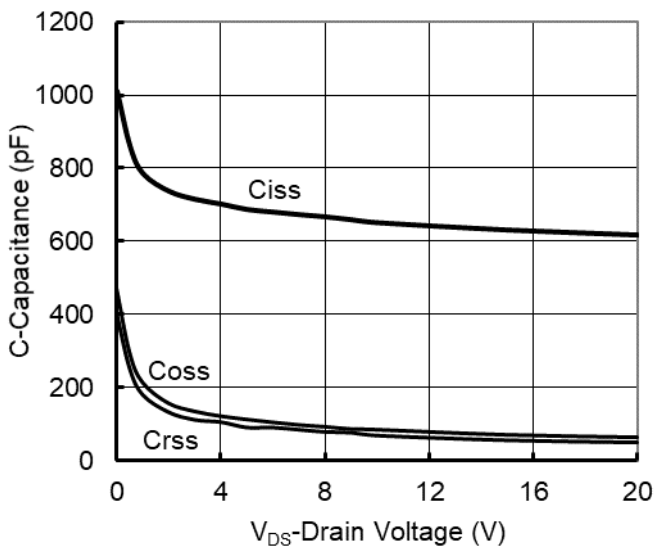


Figure5. Capacitance Characteristics

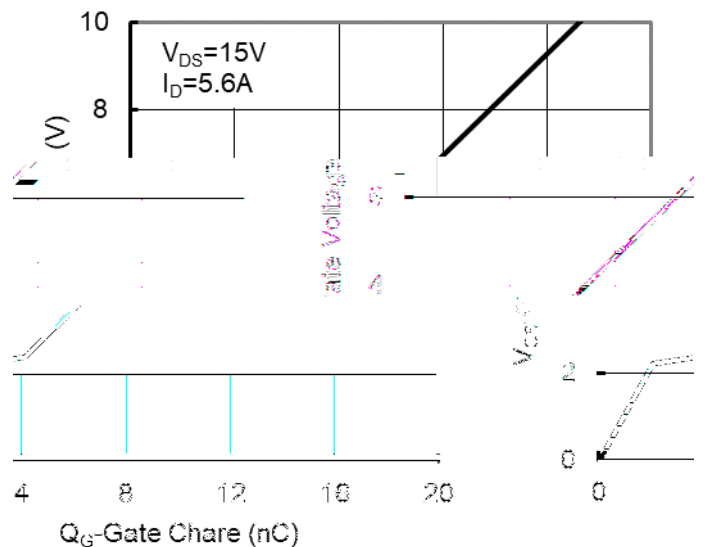


Figure6. Gate Charge



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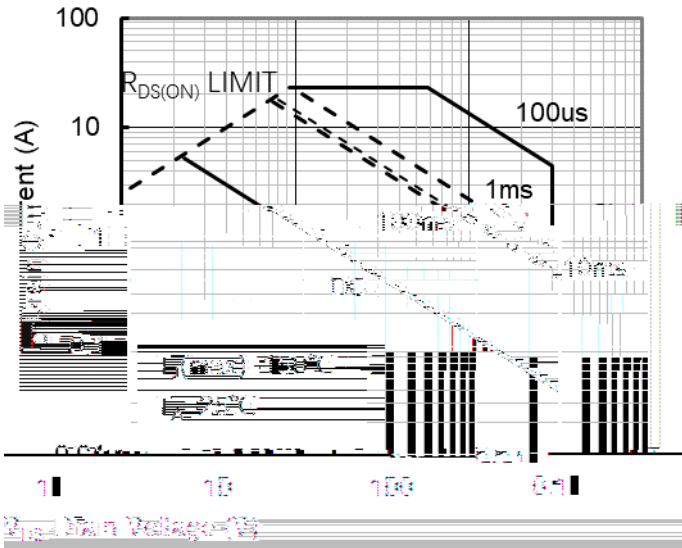


Figure 7. Safe Operation Area

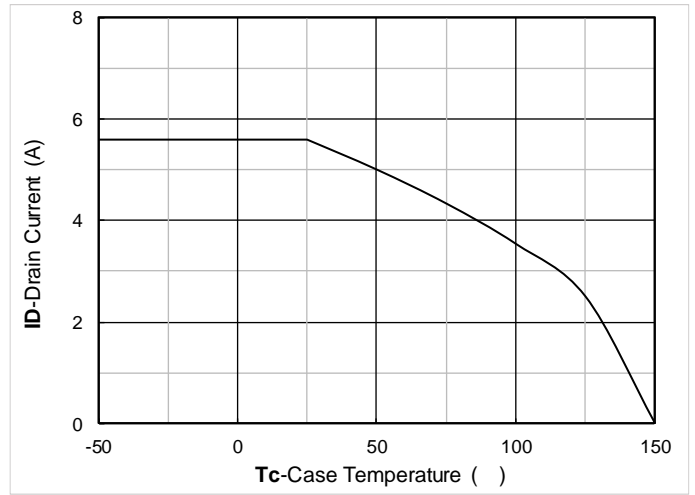


Figure 8. Current dissipation

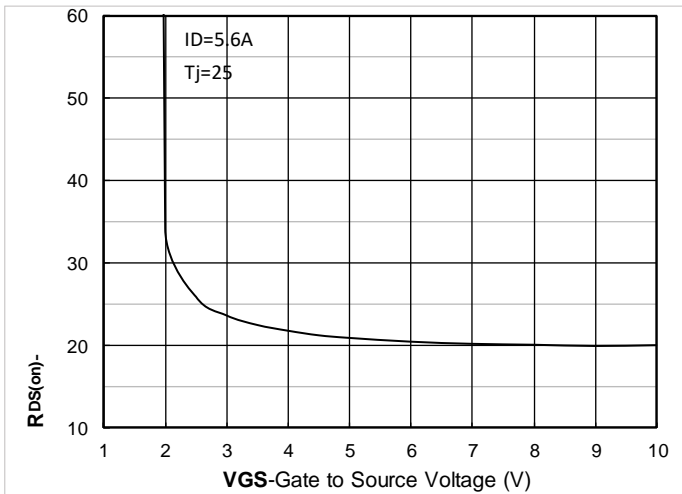


Figure 9. On-Resistance vs Gate to Source Voltage

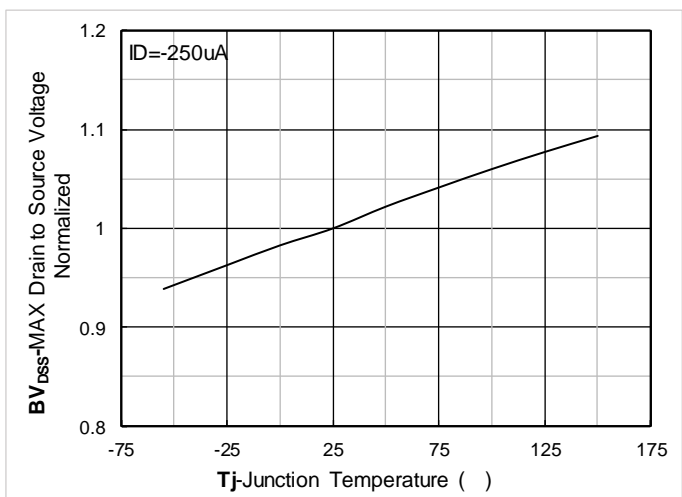
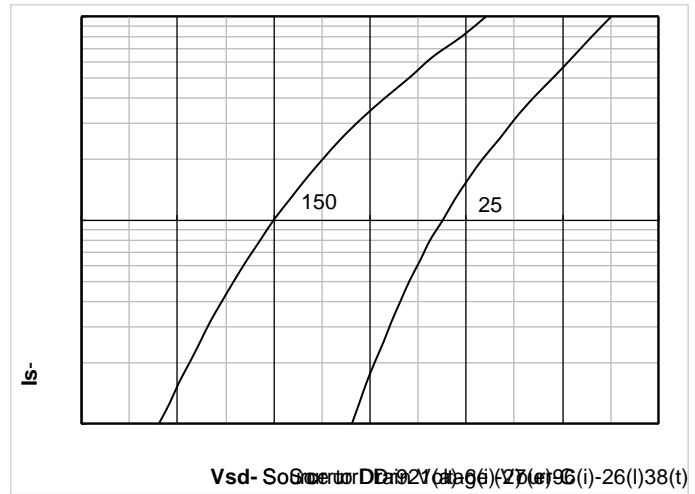
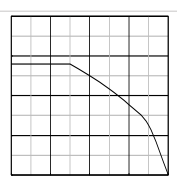


Figure 11. Normalized breakdown voltage





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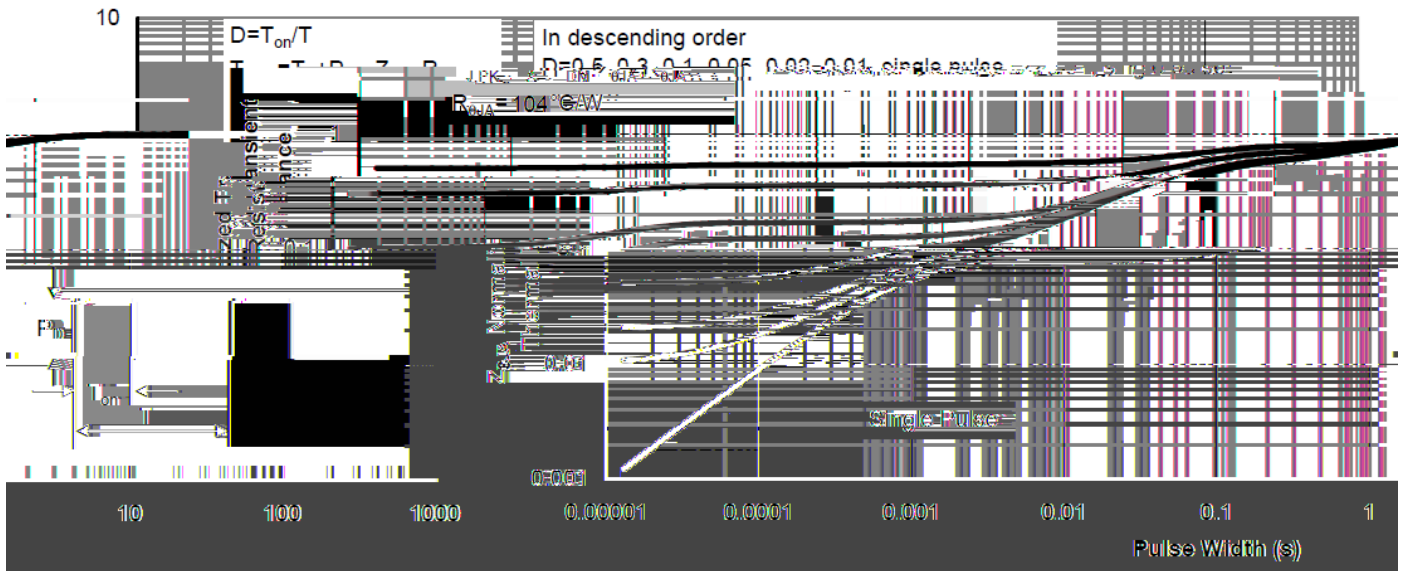
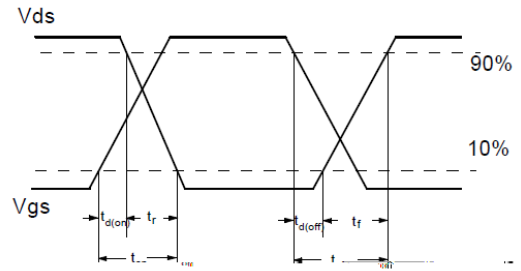
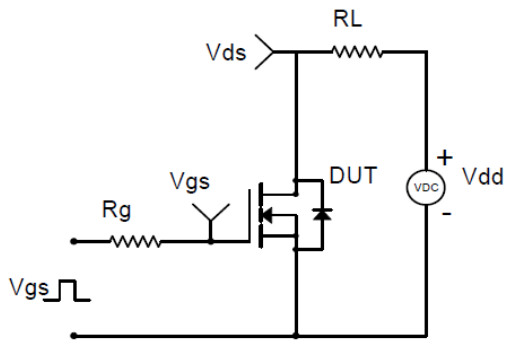
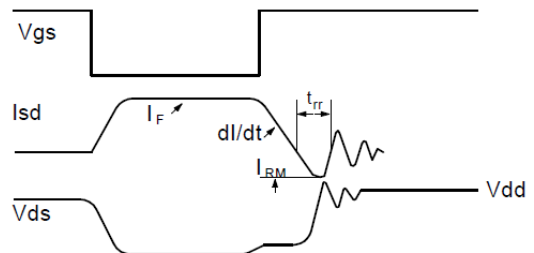
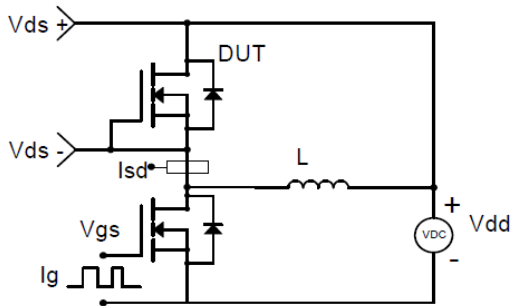


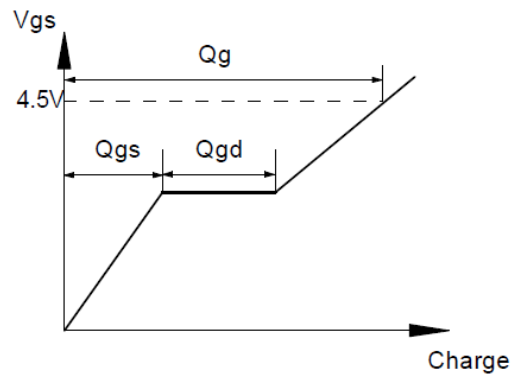
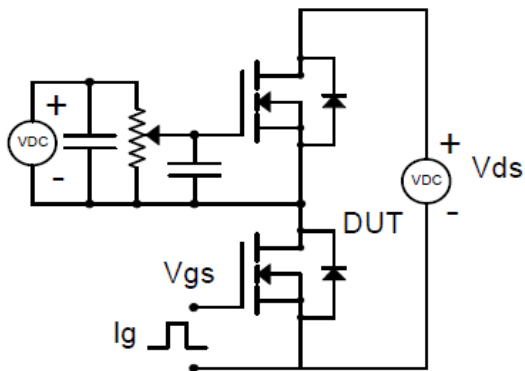
Figure13. Normalized Maximum Transient Thermal Impedance



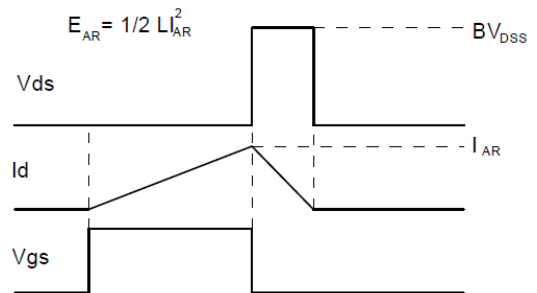
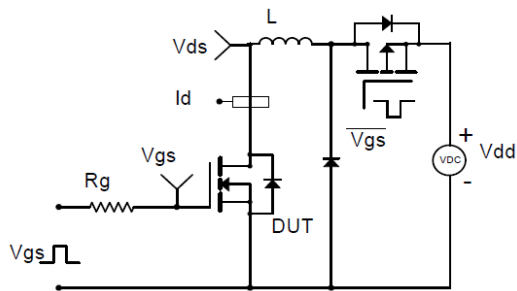
Resistive Switching Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



Gate Charge Test Circuit & Waveform



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



SOT-23 Package information





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